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Research on High Frequency Low-Level System Technology of Accelerator

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Abstract

The 300MeV proton and heavy ion accelerator was independently developed and designed by the Institute of Modern Physics, Chinese Academy of Sciences. The device was a combination of ECR ion source, linear injector and synchrotron. The linear injector consists of seven pulsed high-frequency systems, including one set of RFQ, four sets of DTL, one set of BUNCHER and two sets of DEBUNCHER. The maximum pulse repetition rate is 10Hz and the maximum duty cycle is 1%. The main function of the high frequency and low-level system is to control the amplitude, phase and frequency stability of the high frequency field in the accelerator cavity, to ensure that the beam can obtain stable acceleration when passing through the accelerator cavity, and to reduce the beam loss. The control system hardware based on FPGA and CPCI bus architecture is used in the linear low level system of 300MeV proton and heavy ion accelerator. IQ quadrature demodulation and Cordic amplitude and phase conversion algorithms are used for PI closed-loop control. Online beam experiments show that the phase stability of the closed-loop system is about ±1°, and the amplitude stability is about ±1%, which realizes the long-term stable and reliable operation of the system.

Keywords

SESRI; Linear injector; Low-level system; IQ quadrature demodulation; Cordic

1. Introduction

A Heavy Ion Linear Accelerator is a particle accelerator that accelerates charged heavy ions (atomic number greater than 2, such as helium, oxygen, nitrogen, argon, iron, bismuth, uranium, etc.) to high energies along a straight-shaped track using a high-frequency electric field in a resonant cavity. This kind of accelerator has the advantages of easy injection and extraction, high beam intensity, high transmission efficiency, good quality, and energy can be increased step by step. It is mainly used to generate high-quality heavy ion beams with certain energy by artificial means.

At present, the 300MeV proton and heavy ion accelerator is the core device of the

national "12th Five-Year Plan" major scientific and technological infrastructure SESRI (Space Environment Ground Simulator), which provides a ground simulated irradiation source for the study of the interaction between ion radiation and materials, devices and living organisms, and provides an advanced experimental platform[1] for the basic research of space science and space technology in China. The linear injector of the device is composed of one set of four-rod RFQ accelerator, four sets of IH-DTL accelerator, one set of BUNCHER, two sets of DEBUNCHER and beam transmission lines of each energy segment. Seven high frequency accelerator units were used to accelerate the proton and heavy ion beams to 5.6MeV and 2MeV, respectively, at a frequency of 108.48MHz, a maximum pulse width of 1ms and a maximum repetition rate of 10Hz. Each accelerator unit is equipped with a low-level RF control system. The low-level RF control system mainly completes the following functions: controlling the stability of amplitude and phase in the acceleration cavity, controlling the frequency of the acceleration cavity, data storage and remote control. The main operating indicators of the low-level control system for linear injector of 300MeV proton and heavy ion accelerator are listed in Table 1:

Table1. Operating parameters of low-level control system for linear injector of 300MeV proton and heavy ion accelerator

Project	Index	Project	Index
Cavity field amplitude stability	⩽1%	Cavity field phase stability	⩽±1°
RF output signal form	Pulse	Repetition frequency	⩽10Hz
RF pulse width	⩽1ms	RF output signal frequency	108.48MHz
ADC sampling clock frequency	108.48MHz	Medium frequency	27.12MHz

2. Development Status of Low-Level Control System

Low level control originated in radio broadcast technology, which matured in the second half of the 1920s, and was first applied to charged particle acceleration in 1927, using a drift tube to achieve low frequency (1MHz) acceleration. In the 1930s, radio broadcast technology was further developed to reach high frequencies and high-power levels, allowing particle accelerators to make extensive use of radio frequencies. In the 21st century, with the construction of the Scattered Neutron source in the United States, the Proton Accelerator research facility in Japan), the Shanghai Synchrotron Radiation Light source and the European Free Electron laser project, the low-level control technology ushered in a rapid development, among which the representative is the Lawrence Berkeley Laboratory in the United States (and the German Electron Synchrotron Radiation Laboratory in Germany).

(1) Development of low-level control technology in LBNL

LBNL takes the lead in applying the digital low level system to the accelerator device in the SNS project in the United States. The linear accelerator of SNS consists of RFQ, drift tube linear accelerator (DTL), coupled linear accelerator (CCL), and superconducting accelerator (SCL). The single power source single cavity feeding mode is adopted, and a total of 96 sets of high-frequency systems are used. Each high fre-

quency system includes a power source, high frequency cavity and the digital low level control system, high frequency is 402.5 MHz, frequency conversion under the analog front end for 50 MHz, ADC sampling frequency for 40 MHz. The LCLS-II project of Stanford Linear Accelerator Center and the PIP-II project of Fermilab have been cooperated to develop the low level control system. LBNL digital low-level system adopts the form of a single computer box network port. The analog front end and digital processing are separated in the chassis, and the host computer communicates with each other through Ethernet. This kind of low-level control system in the form of a single computer box is still widely used.

In the LCLS-II project, the superconducting line contains 35 cryostat, each of which has eight 9-ball chambers, and each chamber is individually fed power from a 3.8 kW solid-state power source. In order to further improve the accuracy, LBNL improved the single-chassis architecture to the multi-chassis separately processing architecture, as shown in Figure 2.1. Each half of the cryostat (4 cavities) uses 1 Precision Receiver Chassis (PRC) and 2 RF Station chassis (RFS) for low level control. The critical signals that affect the closed-loop accuracy (such as cavity sampling signals and phase reference signals) are processed in the PRC, and the other signals (such as cavity incident and reflected signals) and loop control are processed in the RFS to reduce the interference between signals in the receiver link. The RFS chassis is shown in Figure 2.1(b).

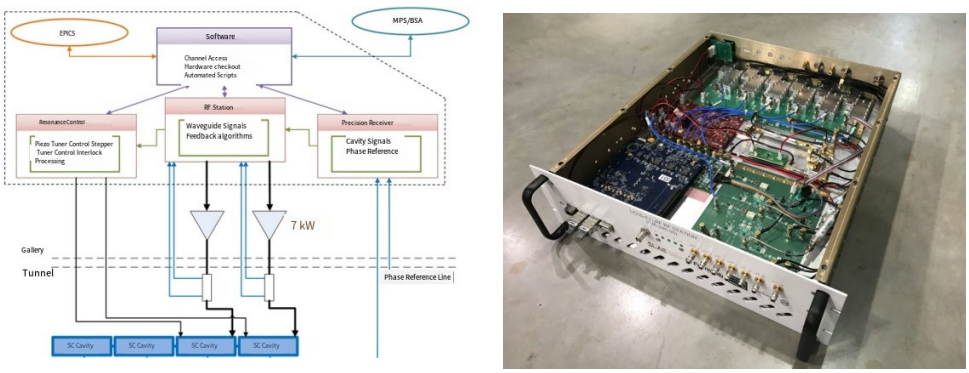

Figure 2.1.LCLS-II Low level control system (a) Low level control scheme (b) RF station chassis

(2) Development of DESY low level control technology

DESY Laboratory has developed low level control systems for FLASH, European XFEL and other projects. The IQ vector and control method are proposed for multi-cavity feeding of a single power source. Taking Eu XFEL as an example, the device consists of 25 high frequency stations, each of which is composed of 4 cryostat (each of which contains 8 superconducting chambers), a 10MW kspeed power source and a set of low level control system. The low-level control system architecture is shown in Figure 2-2 (a), the operating frequency is 1.3GHz, the high-frequency signal is down-converted to 54MHz IF signal through the analog front-end, and the ADC sam-

pling clock is 81.25MHz. The control method based on digital IQ vector sum is adopted, and the feedforward and feedback control methods are used in the loop control. DESY is devoted to the modularization of the hardware platform. Based on the Micro TCA architecture, DESY has launched a series of functional boards such as DS8VM1 and SIS8300, as shown in Figure 2-2 (b), which can help users quickly build a hardware platform. DESY hardware platform has been used in European ESS project and Chinese ADS injector I project. At the same time, projects such as J-PARC in Japan and SNS PPU in the United States have independently developed digital low-level systems based on Micro TCA architecture.

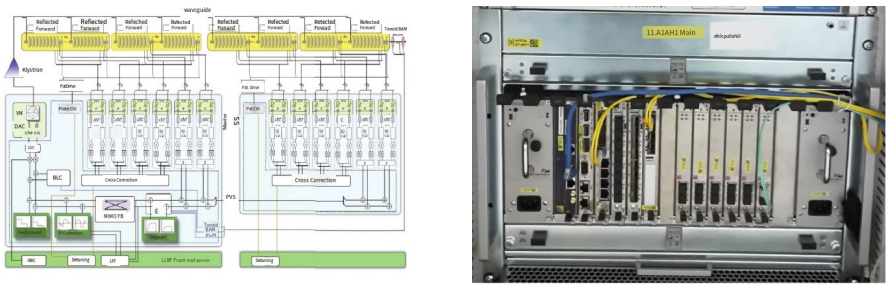

Figure 2-2. European XFEL low level control system (a) Block diagram of low-level control system (b) based on MicroTCA low level controller

(3) Development of domestic low level control technology

The domestic Shanghai Light Source (SSRF) project has carried out the development of digital low-level system earlier. Based on the LBNL scheme, SSRF adopts a digital signal processing platform based on FPGA, and uses the Ethenet interface based on TCP/IP protocol to complete data communication. In order to save cost and development time, the commercial digital signal processing development board which integrates FPGA and AD/DA from A1tera company is selected. The whole system was put into use in 2007. Institute of High Energy Physics has carried out low-level system development in China Hash Neutron source, BEPCII, ILC and other projects. Liu Rong et al. introduced MicroTCA architecture in CiADS Injctor I project. In the CiADS Injctor II project, the Institute of Modern Physics began to develop linear digital low-level system.

Table 2. Low Level RF Control for Electron and Proton Accelerators

	SNS	LCL-II	EuXFEL	ESS
Particle	Proton	Electron	Electron	Electron
Operating frequency	324MHZ	1.3GHZ	1.3GHZ	352.21/704.42 MHz
Power Source	Klystron	Solid state	Klystron	Klystron
Feed mode	Single power source single cavity	Single power source single cavity	Single power source multicavity	Single power source multicavity

Control method	IQ	Vectors and Control	Vectors and Control	Vectors and Control
Medium frequency	50MHZ	20MHZ	50MHZ	50MHZ

In general, the low leIn generalIn general, the low level control technology are usually made of electron accelerator and proton accelerator leads development, as shown in table 1-1, grade two core parameters from rf frequency and power, electron and proton accelerator on the one hand, the working frequency of the radio frequency is high, the typical frequency of 1.3 GHz respectively and 324 MHz, adopts heterodyne architecture, The relatively high RF frequency is down-converted to the intermediate frequency and then digitized, and then directly up-converted to output as an excitation signal to the power source after digital signal processing. Look from the power level on the other hand, the spectrum is mainly selects the klystron power source, the output power can exceed megawatt, can choose the single power source the cavity configuration, such as SNS, also can choose single power source cavity configuration, such as European XFEL.

In contrast, heavy ion linacs have the following characteristics: (a) radio frequency (RF) working frequency is low, the typical frequency of 108 MHz and 162.5 MHz respectively, can be used in a classic superheterodyne structure architecture, such as HIAF 162.5 MHz linear accelerator choose 25 MHz intermediate frequency digital processing, but with the development of electronic technology, direct RF digital architecture is also possible, For example, FRIB 162.5MHz linac; (b) This frequency band even uses multiple solid-state power source single cavity configuration, mainly tube and solid state power source, the output power is 100 kW level, usually adopts single power source single cavity configuration, and with the development of solid-state power source technology and cost reduction, there is a trend to replace tube power source in the future; (c) need to accelerate different ions, mass-to-charge ratio from

1.0 to 7.0, the high frequency electric field requires a large dynamic range, and the influence of the nonlinear characteristics of the high-power solid state power source must be considered in the high dynamic range; (d) flexible and configurable requirements.

Table 3. Low Level RF Control for Heavy Ion Linac

		FAIR-Ulinac	HIAF-iLinac	FRIB	RAON
Operating frequency		108.408MHZ	81.25/162.5MHZ	1.3 GHZ	352.21/704.42 MHz
Power Source		Vacuum tube	Solid state	Vacuum tube	Solid state

Feed mode		Single power source single cavity	Single power source single cavity	Single power source multicavity	Single power source single cavity
Control method		amplitude and phase	amplitude and phase	amplitude and phase	amplitude and phase
Hardware platform		MicroTCA	Single-box network port	Single-box network port	Single-box network port
Sample mode		Direct RF undersampling	Down-conversion intermediate sampling	Direct RF undersampling	Direct RF undersampling

Heavy ion LINac can use the same low level control technology as proton accelerator, but different characteristics lead to different trends in the development of heavy ion low level control technology. Table 1-2 describes the low-level systems used in some heavy ion linacs, among which the representative is the low-level system of FRIB project, as shown in Figure 1-8. Figure 2-3 (a) is the control scheme, and the sampling is direct RF undersampling. Figure 2-3 (b) shows the hardware control platform, which adopts the independent chassis network port platform.

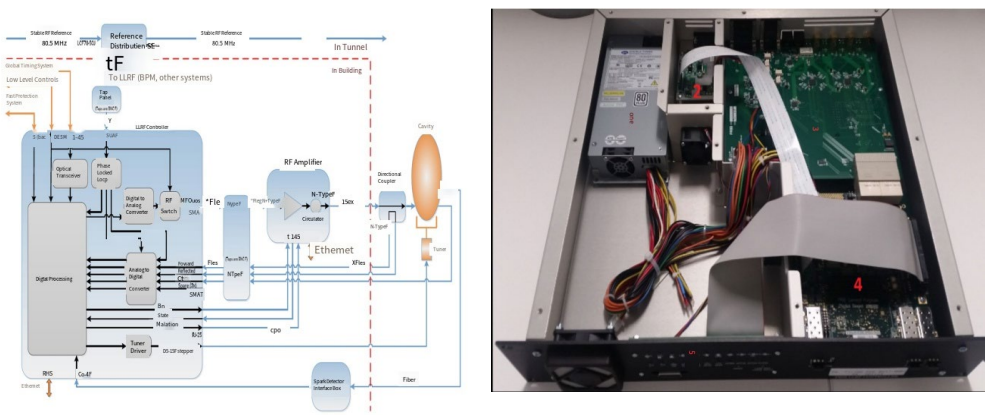

Figure 2-3.FRIB low level control system (a) Low level control scheme (b) independent network port low level control chassis

3. Introduction of Low-Level RF Control System

The low-level RF control system of the linear injector needs to control the amplitude and phase of the high frequency field of the accelerating cavity within ±1% and ±1º, respectively.

The main control board of the low-level RF control system uses a hardware platform based on FPGA+CPCI bus architecture. The ADC and DAC sub-boards communicate with the FPGA main board through high-speed FMC interface. As shown in Figure 3-1, the 108.48MHz RF signal coupled from the cavity is introduced into

the down-conversion module through the attenuator, and mixed with the 81.36MHz Local Oscillator (LO) signal inside the down-conversion module to the Intermediate Frequency (IF) signal of 27.12MHz. After filtering, it is sent to a 14-bit ADC, and the signal sampled by the ADC is processed digitally in the FPGA. After processing, the modulated signal is sent to the DAC to generate an analog 27.12MHz IF signal, and then the signal is introduced to the up-conversion module. Then the signal is mixed with 81.36MHz local oscillator signal to 108.48MHz RF signal output, and the output RF signal is sent to the high-frequency power source for amplification. Finally, the power transmission system is fed into the high-frequency accelerating cavity to form a closed-loop control loop, and the stability of the high-frequency cavity field amplitude and phase is realized. [2-3] In order to achieve the stability of the high-frequency field frequency in the acceleration cavity, as shown in Figure 3-1, the ADC collects two signals, which are the cavity sampling signal of the high-frequency acceleration cavity and the fixed even sampling signal of the cavity incident. These two digital signals are sent to the FPGA, and the phase difference of the two signals is calculated by digital phase identification. The cavity tuner driver module controls the servo driver to adjust the cavity tuner servo motor according to the output direction, pulse and enable control signal of the phase difference signal. At the same time, the limit and position information of the servo motor are fed back to the upper computer control interface for display. The AD9516 clock distribution unit receives an external clock signal of 108.48MHz, and produces a high quality and low jitter clock signal as the working clock frequency of the ADC and DAC. The physical hardware diagram of the low level RF control system is shown in Figure 3-1:

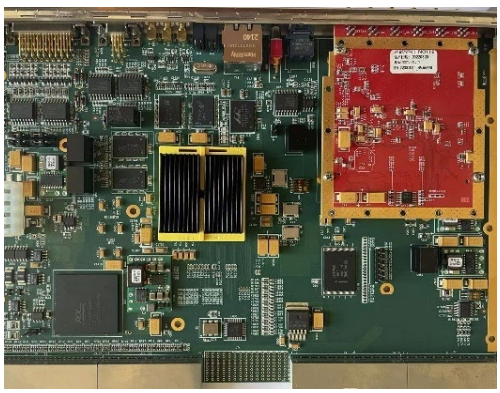

Figure 3-1. Low level RF control system hardware physical diagram

The IF signal sampled by the ADC (27.12MHz) is processed by digital signal processing inside the FPGA. The ADC receives 108.48MHz clock signal generated by AD9516 as its working clock, and the cavity sampling signal and the cavity incident

fixed even sampling signal after down-conversion are sampled by 4 times frequency. That is, the IF signal is sampled 4 times in one cycle, and the sampling point interval is 90°. Assuming that the sampling time is t0, t1, t2 and t3, the sampling value at t0 is the I signal of the current cycle, the sampling value at t1 is the Q signal of the current cycle, the sampling value at t2 is the -I signal of the current cycle, and the sampling value at t3 is the -Q signal of the current cycle. Each group of I, Q, -I, -Q data is stored in registers by means of a 2-bit counter in FPGA. FPGA performs IQ digital demodulation on the sampled data, and set the output of ADC sampling as s(0),s(1),s(2),s(3),... According to equation (1), the separate I and Q can be obtained, and the DC bias in the sampled data can be removed.

Due to the jitter of the system clock, the influence of the power supply noise and the harmonic mixing of the IF signal, the digital I/Q demodulation of FPGA will appear some singular values, which is very unfavorable for the subsequent signal processing. Therefore, the CIC filter of monopole sampling is used to complete the smooth filtering of the I/Q two signals. [4] FIG. 3-3 shows the real-time figure of ADC waveform acquisition and IQ demodulation online operation simulation.

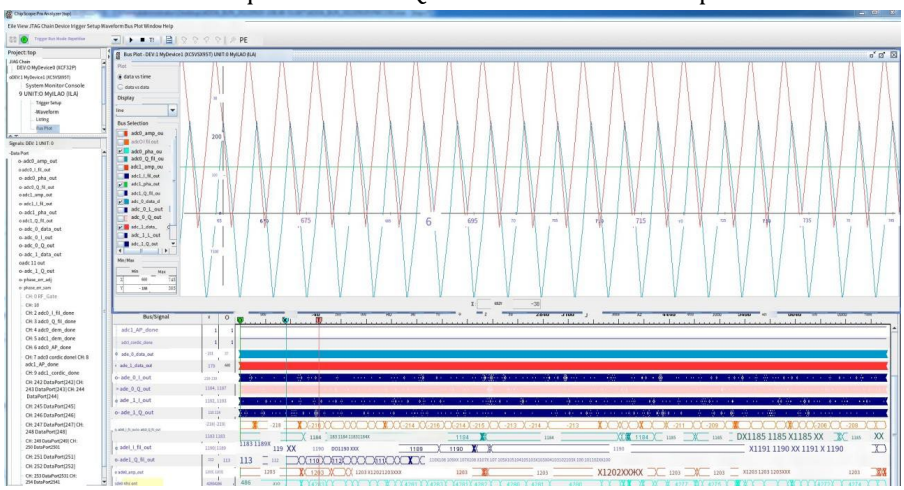

FIG. 3-2. DC acquisition waveform and IQ demodulation online operation simulation diagram

The amplitude and phase information of the IF signal are calculated by the Cordic algorithm inside the FPGA after the two channels of CIC smooth filtering. The amplitude and phase information are respectively entered into the amplitude and phase PI loop inside the FPGA, and finally output by the DAC to realize the stability of the high frequency field of the accelerator cavity. PID(Proportional Integral Derivative) control is one of the earliest developed control strategies. Because of its simple algorithm, good robustness and high reliability, it is widely used in industrial process control. The same control module is used in I/Q two channels, the input data is 16, and the set data is 16. The output of controller is 16 bits.

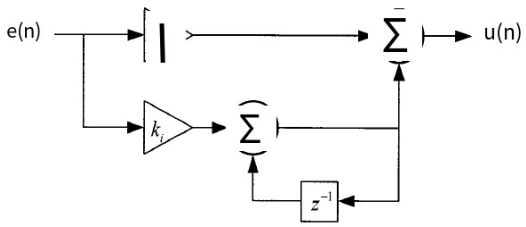

Figure 3-3.PI loop control block diagram

The host computer control interface adopts the EPICS IOC framework, which provides important interactive information interface, realizes relevant data processing and algorithms, and provides alarm and remote control. The software mainly includes amplitude and phase control, RF protection, movable tuner and other display and control interfaces. Through the software interface, the visualization functions such as cavity field waveform display, amplitude and phase setting, open-loop and closed-loop control, automatic frequency conversion, PI feedback parameter tuning, RF protection parameter setting and so on are provided. The control interface of the host computer is shown in Figure 3-4.

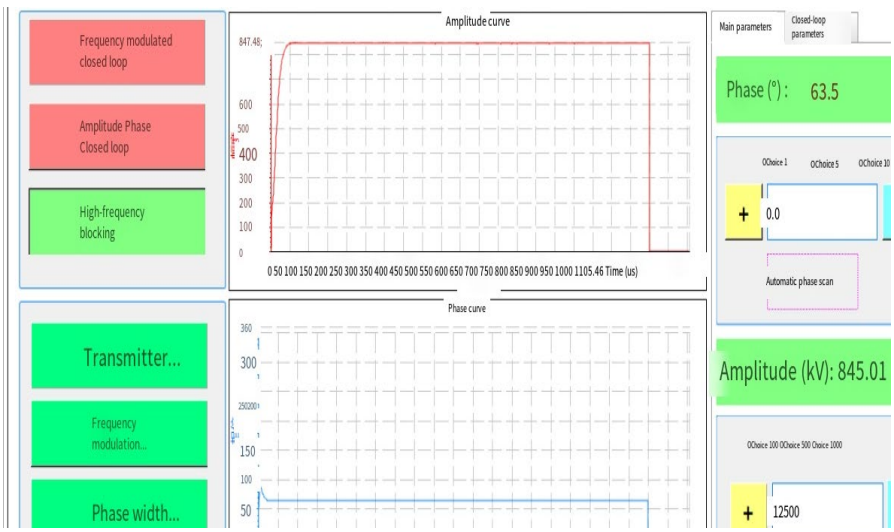

Figure 3-4 Control interface diagram of the host computer

4 Run the test online

The linear injector of 300MeV proton and heavy ion accelerator can accelerate all the stable nuclide beam. After long-term operation, the high-frequency low level RF control system of the linear injector runs stably and reliably for a long time. The closed-loop phase stability in the acceleration chamber is about 1°, and the amplitude stability is about ±1%. H_2+Bi^(32+)The sampling waveforms of RFQ, DTL1, DTL2 and BUNCHER cavities in the low-level closed-loop state are shown in Figure 3-5 below.

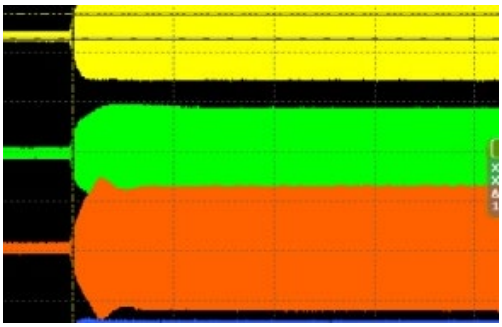

Figure 3.5 Cavity Sampling Waveform (closed-loop state)

5. Summary and Prospect

Summary: The high frequency and low-level RF control system for linear injector of 300MeV proton and heavy ion accelerator is based on hardware platform of FPGA and CPCI bus architecture. IQ orthogonal demodulation is used in algorithm, Cordic algorithm is used for amplitude and phase conversion, and PI algorithm is used for closed-loop control. The online performance index is better than the design index, and the long-term operation is stable and reliable.

Outlook: The development of digital low-level system is a process of continuous iterative improvement. Although this paper has achieved preliminary research results, there are still some shortcomings, which need to be further explored and improved in the follow-up research.

The following are some directions for future research:

(1) Optimize the digital low level control platform: The digital low level control platform needs to be further optimized, especially around the 250 MHz ADC high-precision sampling and 500 MHz DAC output. Upgrade the ADC to AD9467 and the DAC to AD9747, cancel the FMC interface, and optimize the clock layout and external interface to further improve the system performance.

(2) Research on real-time digital pre-correction technology based on FPGA: In this paper, the third-order polynomial model of solid-state power source is constructed in the host computer by using the floating point arithmetic ability of CPU, and the dynamic adjustment of loop gain is realized to realize nonlinear correction. However, this method cannot be applied to heavy beam loads and feed-forward loops. Therefore, FPgas based real-time digital pre-correction techniques need to be studied to better cope with these challenges.

(3) Further research on direct RF digitization architecture: direct RF digitization architecture represents the future development direction. In order to achieve higher accuracy, more advanced research and experimental platforms, high performance instruments for clock and ADC chip testing are needed. This includes high performance signal generators, signal analyzers, and filters for various signals. While these conditions will take time to establish, they will pave the way for the development of

direct RF digitization architectures.

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