

# Design and Implementation of an FPGA-Based Data Acquisition System for Accelerator Synchronous Power Supply

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## Abstract

In synchrotrons, the quality of beam acceleration depends on precise control of the composite magnetic field, which requires multiple sets of magnet power supplies to achieve accurate synchronization. Therefore, multi-channel synchronous acquisition of magnet power supply signals is a key step in evaluating their actual synchronization performance. However, the existing power supply acquisition system of CSRm suffers from issues such as complex structure and large volume. To address the synchronization requirements and system upgrade needs of the acquisition system, a synchronous multi-channel data acquisition system scheme is designed. The system consists of an AD acquisition module and a logic processing module. The AD acquisition module performs synchronous acquisition of multiple sets of power supply signals. The logic processing module, based on the FPGA of the ZYNQ platform, handles data transmission and filtering; the ARM side runs an embedded Ubuntu system and, together with the driver, achieves functional control and data transmission of the acquisition system. Finally, module functions and indicators of the acquisition system are tested. The test results show that the acquisition frequency remains stable above 9999 Hz, and the time difference between two channels is stable around 1  $\mu$ s, meeting the accelerator channel requirement of less than 5  $\mu$ s delay, thus verifying the feasibility of the system.

## Keywords

Data Acquisition; ZYNQ Soc; Embedded Linux; Digital Filter

## 1. Introduction

In a synchrotron, the control of the beam orbit depends on the composite magnetic field generated by the coordinated action of multiple magnets (e.g., dipole and quadrupole magnets)[1][2]. The precise establishment of this composite magnetic field requires each magnet's independent power supply to accurately control its

excitation current. The synchrony of the excitation currents directly determines the synchrony of the magnetic fields, which in turn affects the beam orbit accuracy and acceleration efficiency [3]. To accurately monitor and evaluate the actual synchronization performance of each independent power supply during operation, it is necessary to eliminate the time errors artificially introduced by asynchronous signal sampling. Therefore, multi-channel synchronous acquisition of signals from multiple magnet power supplies is required to truthfully represent the dynamic synchronization characteristics of each power supply current. The existing magnet power supply acquisition system has a working sampling rate of 5 kHz. When testing the synchrony of the power supplies, the system operates at a sampling rate of 1 MHz, and the synchronization performance requirement for the acquired signals is that the inter-channel delay shall not exceed 5  $\mu$ s.

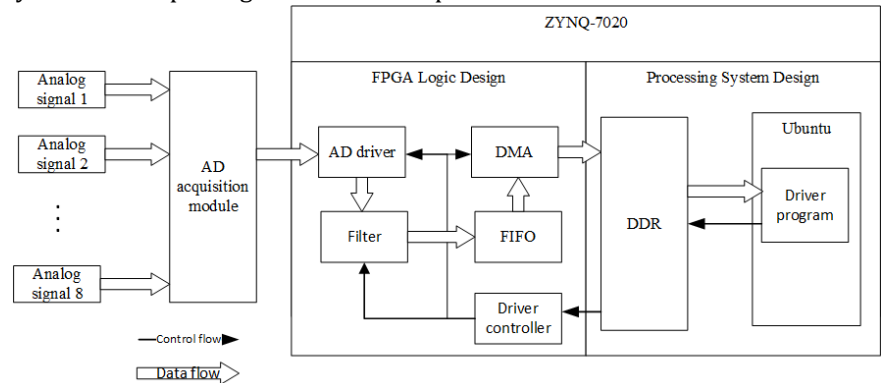
The existing power supply acquisition system at HIRFL-CSRm is based on the PXI architecture. Its chassis is an 18-slot PS6040-PXI-18, with an ADLINK PXI-3800 main controller installed in the left slot and an NI PXI-6133 multi-channel data acquisition board inserted in the right slot [3]. However, with the continuous evolution of acquisition system architectures, the limitations of this system have gradually become apparent: it requires a combination of multiple hardware components such as a chassis, a controller, and acquisition cards, leading to structural complexity, low integration, a large overall volume, and significant occupation of rack space. In contrast, System-on-Chip (SoC) technology, which highly integrates various functional modules onto a single chip [13], can effectively address the above issues. Based on the above analysis, this paper adopts a Zynq SoC board [4], which features high scalability, heterogeneous characteristics, and broad hardware compatibility, together with an AD acquisition module, to design a new high-speed data acquisition system for synchrotron power supplies. This architecture significantly improves system integration and reduces cost. Furthermore, an Ubuntu operating system is deployed in the ARM processor of the ZYNQ, enabling program compilation and execution directly on-chip, thereby simplifying the tedious cross-compilation environment configuration steps that are typically required in traditional ZYNQ development workflows.

## **2. System Framework and AD Acquisition Module Design**

### **2.1. System Framework Design**

The framework of the designed system is shown in Figure 1. The system consists of two main parts: the AD acquisition module and the logic processing module. The AD acquisition module performs synchronous acquisition of 8-channel analog signals. The logic processing module is developed and designed based on a ZYNQ 7000 series board. The programmable logic (PL) and the processing system (PS) are the two major components of the ZYNQ 7000 series board [5][6]. In this system, an AD driver unit, a decimation filter unit, a DMA transfer component, and a FIFO buffer

component are designed on the PL side. On the PS side, an embedded Ubuntu system is set up along with the development of relevant drivers.



**Figure 1.** Overall system architecture diagram.

The AD acquisition module first completes the synchronous acquisition and analog-to-digital conversion of multi-channel analog signals. The converted digital signals are buffered by a FIFO and then sent to the DMA module. The driver running on the PS side controls the decimation filter unit, allowing selection between the 1 MHz sampling mode or the 5 kHz digital filtering mode. Subsequently, the driver controls the DMA to transfer the data via a high-speed bus to the DDR memory on the PS side for buffering, and finally reads and saves the acquired data under the Ubuntu operating system running on the PS side.

## 2.2. Hardware Design of the AD Acquisition Module

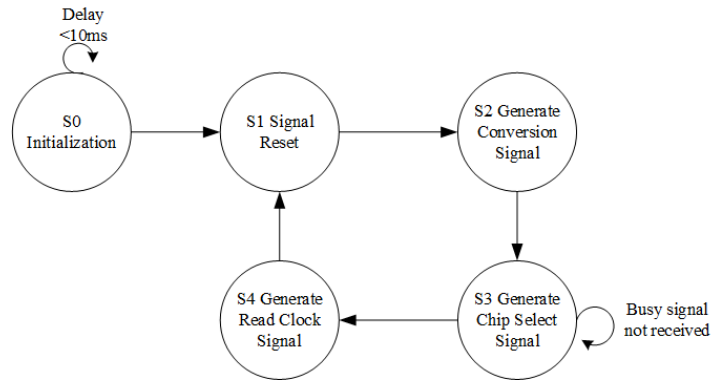
According to the accelerator magnet power supply signal acquisition specifications shown in Table 1, this system selects the AD7606C-16 from Analog Devices as the analog-to-digital converter chip. This chip operates from a single 5 V supply, supports 8-channel synchronous sampling, and achieves a maximum sampling rate of 1 MS/s per channel, meeting the multi-channel and sampling rate requirements. In parallel transmission mode, the theoretical minimum inter-channel acquisition delay is only 15 ns, which is far superior to the 5  $\mu$ s specification required by the existing system. Additionally, the AD acquisition module integrates an input protection circuit to achieve reverse polarity protection for the power supply.

## 3. FPGA Logic Design

### 3.1. Design of the AD Driver Unit

Based on the AD module hardware, an AD driver unit was designed on the Vivado platform to implement the parallel interface timing of the AD7606C-16 for driving AD acquisition. The key states of the AD7606C-16 parallel interface timing are as follows: When the CONVST pin transitions from low to high, an analog-to-digital conversion is initiated; the BUSY pin outputs a high level at the

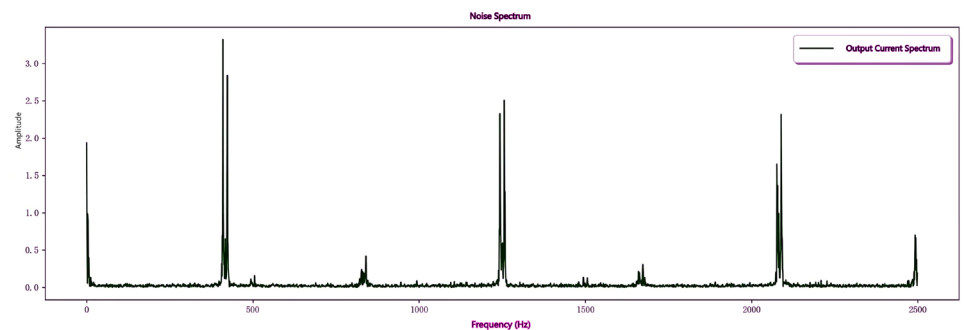
start and end of the conversion. While both the chip select (CS) and read enable (RD) pins are active low, data are read out sequentially from channel 1 to channel 8. The state flow is shown in Figure 2.



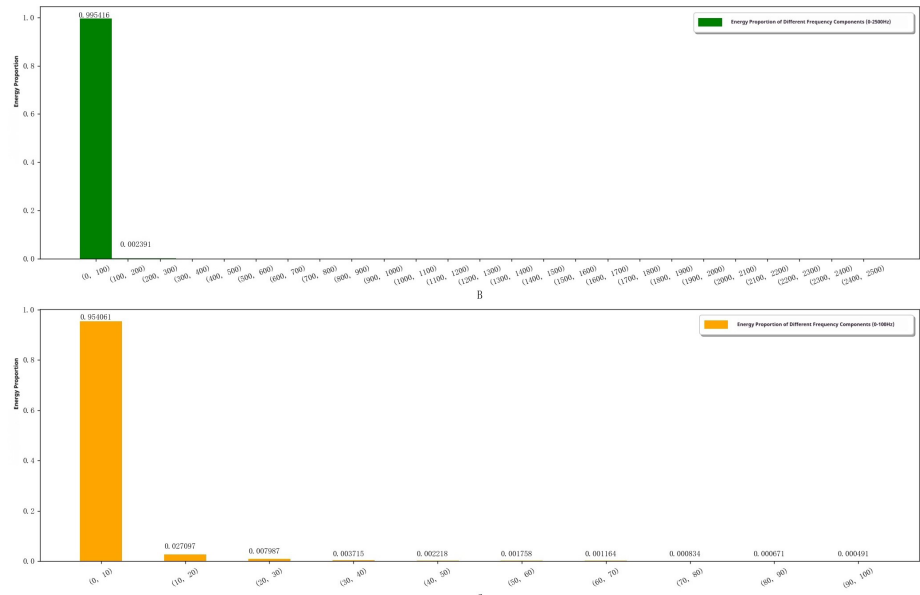
**Figure 2.** Flowchart of acquisition timing states.

### 3.2. Design of the Decimation Filter Unit

There are different sampling rate requirements for the power supply signals in the CSRm facility. Based on this situation, the proposed system implements a 5 kHz sampling mode, which is obtained by decimating the 1 MHz signal according to the frequency ratio. Furthermore, digital filtering functionality is extended on top of the 5 kHz sampling mode. The design of the 5 kHz digital filter module includes two aspects: filter design and hardware implementation. For filter design: the ambient noise power spectrum (as shown in Figure 3) is obtained by processing the field data sampled at 5 kHz, and the ideal power supply signal power spectrum (as shown in Figure 4) is analyzed. The analysis indicates that the field noise is mainly concentrated in the high-frequency band near and above 417 Hz, while the energy of the ideal power supply signal distributed in the range of 0–100 Hz reaches 99.5%.



**Figure 3.** Noise spectrum of the dipole power supply.



**Figure 4.** Power spectrum of the ideal power supply signal.

Based on the above analysis, this system adopts a fourth-order filter formed by cascading second-order IIR digital filters in direct form Type II. Compared with the direct form Type I structure, the direct form Type II offers significant advantages in saving hardware resources, while the cascaded structure is easy to implement and less affected by parameter quantization [7]. According to this structure and parameters, a filter that meets the passband and stopband gain requirements is designed using the Matlab Filter Design Toolbox.

In terms of hardware implementation: the coefficients of the IIR digital filter must be quantized during hardware implementation [8]. Therefore, this system performs 24-bit signed integer quantization on the coefficients obtained from the Matlab Filter Design Toolbox. The quantization procedure first normalizes the coefficients by a power of two ( $Q_m$ ) based on the maximum absolute value of the coefficients, and then linearly maps them onto the entire 24-bit integer range. The floating-point parameters before quantization and the quantized first-section filter parameters are shown in Table 1 below.

**Table 1.** Quantization table of filter coefficients for Section 1.

	b0	b1	b2	a0	a1	a2
floating-point parameter	0.003762	0.007524	0.003762	1.0	-1.893415	0.908464
quantization parameters	24'd1578	24'd3156	24'd1578	24'd419430	-24'd794156	24'd381037
	0	0	0	4	0	5

Finally, on the PL side, the filtering function is implemented by matching the quantized coefficients with the coefficients of the difference equation shown in

Equation 1 and with the delay units at each stage.

$$y(n) = \sum_{i=0}^M x(n-i)b(i) + \sum_{l=1}^N y(n-l)a(l) \quad (1)$$

### 3.3. DMA Transfer Component and FIFO Buffer Component Design

To achieve efficient data transfer, this paper adopts Direct Memory Access (DMA) for transferring data between the FPGA and the ARM processing system. When the system performs 8-channel, 16-bit data transmission, the single transfer data amount is 128 bits, and the maximum sampling frequency is 1 MHz, resulting in a maximum transmission bandwidth of 128 Mbps. Considering data buffering, the transmission method uses AXI DMA, controlled by a CPU interrupt signal. Compared with AXI memory-mapped interfaces, AXI DMA provides a higher-bandwidth direct memory access channel interface [9]. The AXI-HP interface is selected for interaction, which supports a 50 MHz clock and 64-bit data width, offering a transmission bandwidth of up to 3.2 Gbps, meeting the required bandwidth for transmission. Additionally, an AXI Stream FIFO is added on the PL side to enable synchronous data transfer [10].

## 4. Processing System Design

### 4.1. Building of the Embedded Ubuntu System

The PS side of the Zynq chip not only contains an ARM processor but also integrates a set of supporting processing resources internally, which work together to form a complete Application Processing Unit (APU). Regarding the APU, this paper mainly configures the HP interface, I/O peripherals, clock, DDR, and interrupt ports. For extended peripheral interfaces, the QSPI, SD, and UART peripherals are configured. After integrating the developed PL design in Vivado and completing the corresponding PS configuration, the hardware description file including the bitstream is generated through compilation, synthesis, implementation, and pin assignment. The hardware description file is imported into a virtual machine to create a Petalinux project, and the configuration functions of the toolchain are used to set key parameters, including kernel image settings, boot image settings, dtb image settings, and root filesystem type configuration. The compiled BOOT.BIN file and the corresponding root filesystem are integrated into an SD card. After booting the development board from the SD card, the system automatically performs the relevant configuration initialization and setup, thereby completing the construction of the embedded Ubuntu system [11].

### 4.2. Driver Development

The driver is the bridge connecting the user-space program and the hardware. It is responsible for initializing the hardware, configuring parameters, and providing an interface to access the hardware. In the driver, memory mapping functionality needs

to be implemented. In this design, the mmap function in Ubuntu is called to accomplish the interaction between the PS and the DDR memory. By pairing the memory mapping function mmap with the unmapping function munmap [12], data information such as waveform signals and various status values stored in the DDR address can be retrieved and written.

The core driver operation flow of this design is as follows: after the program starts, it first uses the mmap function to map and initialize the DDR memory address, then configures the control registers of the ADC and DMA, and selects the acquisition mode of the system. After starting the ADC and DMA, it polls the value of the DMA status register. Once the DMA return value is obtained (indicating that the DMA transfer is complete), it saves the data and prints the first 64 bits of data, and finally exits the program. If a timeout or interrupt error occurs, it prints an error message and terminates the program.

## 5. Acquisition System Testing

### 5.1. System Module Functional Testing

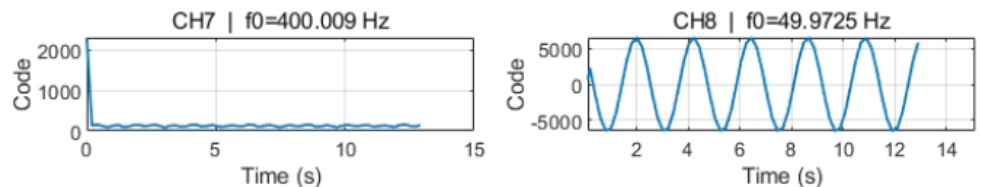
System acquisition test: Using a signal generator as the input, the board and the acquisition card were connected and acquisition was controlled via the serial port. The running results are shown in Figure 5. Data were successfully acquired and the first 64 bits were printed.

```
[TEST 4] AXI DMA + ADC Data Acquisition Test
[STEP] Waiting for DMA transfer...
[SUCCESS] DMA transfer completed!
DMA Buffer Data (first 64 bytes):
13 00 0A 00 10 00 09 00 09 00 18 00 68 FF 8C FF
12 00 0A 00 10 00 09 00 09 00 17 00 67 FF 8C FF
11 00 0A 00 10 00 0A 00 08 00 18 00 67 FF 8C FF
11 00 0B 00 10 00 0A 00 08 00 17 00 68 FF 8D FF

[SUCCESS] Save DDR data to adc_dma_data.txt complete!
[INFO] Saved 1048576 bytes data from 0x10000000
[SUCCESS] AXI DMA + ADC test completed!
```

**Figure 5.** Results of system acquisition operation.

System filtering test: A signal generator was used to input a 50 Hz analog power supply signal into channel 8 and a 400 Hz analog noise signal (the field noise is at 417 Hz and above) into channel 7. The acquired data were processed as shown in Figure 6. Analysis shows that in the filtering acquisition mode, the waveform of channel 7 is filtered as expected after a short delay, while channel 8 completely acquires a sinusoidal waveform, thus achieving the filtering function.



**Figure 6.** Filter function test.

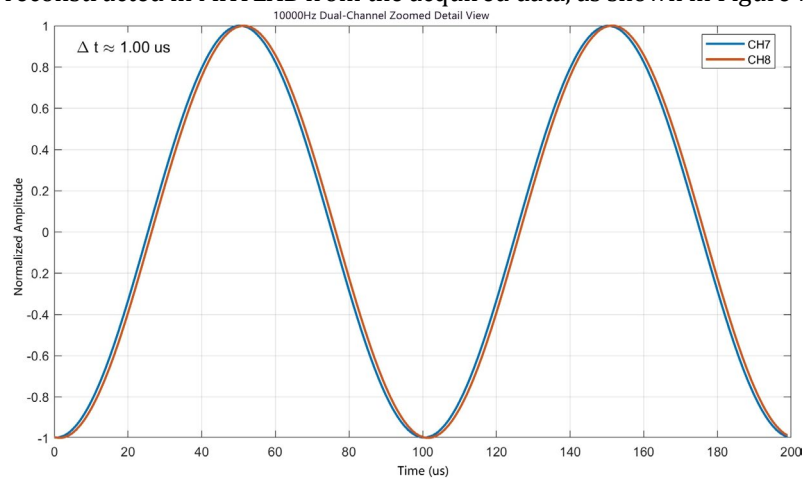
## 5.2. System Acquisition Specification Testing

The test objectives include sampling frequency, synchrony, waveform consistency in the high-frequency acquisition mode, and the filtering function in the filtering acquisition mode. The test environment uses a Tektronix AFG3252 dual-channel arbitrary function generator to provide the required input signals for synchronous acquisition testing. Due to hardware limitations, only the test of synchronous acquisition of dual-channel input signals was performed. The characteristics of the signals used in the test and the acquisition system settings are shown in Table 2 below.

**Table 2.** Test signal characteristics and acquisition system settings.

	Signal Frequency	Signal Amplitude	Signal Waveform	Sampling Frequency	Filter Mode
Channel 7	10kHz	1Vpp	Sine wave	1MHz	Off
Channel 8	10kHz	1Vpp	Sine wave	1MHz	Off

The system is controlled and data is acquired by the host computer via a USB-to-serial port interface using serial port software. Using the test signals from Table 4 as input, the acquired data from the system are saved, and the waveform is reconstructed in MATLAB from the acquired data, as shown in Figure 7.

**Figure 7.** Waveforms of channel 7 and channel 8.

To comprehensively evaluate system performance, MATLAB is used to perform quantitative testing on the saved acquisition data from three dimensions: actual sampling rate, channel synchrony, and waveform consistency. The actual sampling rate is derived by frequency domain analysis of the acquired waveforms. Channel synchrony is characterized by the phase difference of the synchronously input dual-channel signals (channel 7 and channel 8), which is converted into a time difference. Waveform consistency is evaluated using two metrics jointly: the Pearson correlation coefficient is used to assess the similarity between the acquired

signal and the input signal, with values closer to 1 indicating stronger linear correlation; the normalized root mean square error (NRMSE) is used to assess amplitude correlation, with smaller values indicating higher amplitude consistency. Combining the above two metrics allows a comprehensive judgment of the system's waveform acquisition consistency. Some test results are summarized in Table 3.

**Table 3.** Statistics of dual-channel acquisition data.

Test number	1	2	3	4
Time difference (us)	1.000000	0.999999	1.000000	1.000000
Channel 7 actual sampling frequency (hz)	999924.659985	999924.227241	999924.0574941	999923.9817941
Channel 8 actual sampling frequency (hz)	999924.666884	999924.219546	999924.036241	999923.999814
Channel 7 NRMSE (%)	1.595649	1.605185	1.608493	1.610161
Channel 8 NRMSE (%)	1.595909	1.604760	1.607644	1.610986
Channel 7 correlation coefficient	0.999745	0.999743	0.999741	0.999741
Channel 8 correlation coefficient	0.999745	0.999743	0.999742	0.999741

According to the analysis of the table, the actual acquisition frequencies of channel 7 and channel 8 are stable above 9999 Hz, which essentially meets the 1 MHz specification. The NRMSE of both channels is stable in the range of 1% to 2%, indicating that the amplitude of the acquired signal is basically consistent with that of the input signal. The correlation coefficients of both channels are close to 1, indicating that the waveforms of the acquired signals are basically consistent with those of the input signals. The time difference between the two channels is stable at approximately 1  $\mu$ s, meeting the accelerator channel specification of less than 5  $\mu$ s delay.

## 6. Conclusion

This paper addresses the structural optimization requirements of the synchronous magnet power supply acquisition system for the HIRFL-CSRm accelerator. A multi-channel synchronous power supply data acquisition system scheme is designed. The data acquisition system, built around the Zynq-7020 development board and the AD7606C-16 chip, achieves multi-channel synchronous acquisition of output signals from the synchrotron magnet power supply groups and accomplishes a structural upgrade. A digital filter function is also implemented at a 5 kHz sampling rate. Through acquisition testing and data processing analysis, the synchrony, actual sampling rate, waveform consistency, and filtering function of the acquisition system are evaluated, verifying that the system meets all on-site specifications. Compared with the original magnet power supply acquisition system of the CSRm accelerator, this Zynq-based acquisition system with an AD module

offers improved integration and flexibility, while reducing system maintenance costs and expansion difficulty.

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