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Research and Practice on the New Apprenticeship Training Pathway for Integrated Circuit Industry Talents

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Abstract

In response to the shortage of high-skilled talents and the disconnection between traditional training models and industrial demands amidst the accelerated domestic substitution in the integrated circuit (IC) industry, this paper systematically elaborates on a new apprenticeship training pathway characterized by "One Student, One Pathway" and "Primary-Secondary Job Synergy." Based on the mod-ern apprenticeship talent training scheme of Suzhou Industrial Polytechnic, this pathway relies on the "New Factory-in-School" co-built with domestic leading enterprises such as Empyrean, Eswin, and Accotest. It reconstructs a modular curriculum system comprising 20 courses totaling 157.5 credits, emphasizing practical training on domestic EDA tools, domestic test equipment, and domestic chips. By implementing a four-stage progressive training process—"Foundation Consolidation → Core Specialty Construction → Primary-Secondary Job Com-prehensive Practice → Enterprise Post Training"—and establishing a differenti-ated assessment mechanism where the primary job accounts for ≥70% of the weight, the pathway effectively achieves a precise match between student skill growth and enterprise job requirements. Practice shows that this pathway sig-nificantly improves graduates' job adaptability and operational capabilities with domestic tools, providing a replicable paradigm for similar institutions.

Keywords

Integrated Circuit; Modern Apprenticeship; One Student One Pathway; Domestic Substitution; Four-Stage Progression

1. Introduction

The integrated circuit (IC) industry is a strategic, foundational, and pioneering sector supporting economic and social development and safeguarding national security. With the in-depth implementation of the "14th Five-Year Plan" and the advancement of the domestic substitution strategy, there is an urgent demand in

China's IC industry for high-skilled talents capable of operating domestic toolchains and solving complex engineering problems. However, current vocational education talent training faces prominent issues such as curriculum content lagging behind process iterations, training scenarios lacking real production line environments, and singular evaluation standards. These issues result in graduates being unable to directly be competent for enterprise positions, especially those involving domestic equipment operations.

To address this, this study relies on the modern apprenticeship talent training scheme for the IC technology major at Suzhou Industrial Polytechnic. In collaboration with domestic core enterprises such as HX Microelectronics, Accotest, Eswin, and Empyrean, we deepen industry-education integration and innovatively propose a new apprenticeship training pathway featuring "One Student, One Pathway" and "Primary-Secondary Job Synergy." This paper aims to comprehensively analyze the curriculum system reconstruction, the four-stage progressive implementation process, and the diversified evaluation mechanism of this pathway, hoping to provide concrete and operable paradigm references for talent training reforms in IC and related hard-tech majors at other institutions.

2. Logical Starting Point: Curriculum System Reconstruction Based on Job Competency Maps

The core of modern apprenticeship lies in the "integration of work and learning," with the curriculum serving as the vehicle to achieve this goal. This study abandons the traditional disciplinary knowledge system. Instead, taking the competency requirements of five typical job positions in the IC industry chain (Layout Design, Packaging, Testing, Facility Management, and Application Development) as the logical starting point, we draw a dynamically updated "Job Competency Map." Based on this, we have reconstructed a modular curriculum system totaling 157.5 credits across 20 courses.

2.1. Bottom-Layer Sharing: Consolidating General Quality and Professional Foundations

Addressing common industry requirements, we set up 37.5 credits of compulsory public courses and 19 credits of professional foundation courses. In addition to conventional courses such as Ideological and Political Education, Sports and Health, and Advanced Mathematics, we have particularly strengthened vocational basic skills. For instance, the course Soldering Process of Electronic Components (1 credit) introduces IPC international standards with a 0.5-week intensive training session to ensure students master high-reliability soldering skills. EDA Technology and Applications (4 credits), as a course featuring domestic substitution co-built with Sanwei Microelectronics, focuses on cultivating students' ability to use domestic EDA tools for schematic drawing and PCB design, laying a solid foundation for subsequent professional learning.

2.2. Middle-Layer Differentiation: Aligning with Specialized Skills in Sub-fields

Based on the five core job positions, we established 12 credits of professional core courses and 12 credits of professional practical training courses to achieve precise alignment of "one course, one job" or "one course, multiple jobs."

• Layout Design Direction: Offers Fundamentals of IC Layout Design (co-built with Empyrean), focusing on the operation of Empyrean's domestic EDA tools and the design and verification of basic unit layouts such as inverters.

• Packaging Direction: Offers Fundamentals of IC Packaging Technology (co-built with Belai Information), covering key operational points of core processes like wire bonding, molding, and trim/form.

• Testing Direction: Offers Fundamentals of IC Testing Technology (co-built with Accotest). Relying on domestic test equipment, it systematically teaches open/short testing, DC/AC parameter verification, and fault troubleshooting.

• Facility Management Direction: Offers Semiconductor Facility Management, managing HVAC, special gases, ultra-pure water, and power systems in a modular manner to cultivate equipment operation, maintenance, and safety management capabilities.

• Application Development Direction: Offers Fundamentals of MCU Development (co-built with HX Microelectronics) and Introduction to Verilog HDL and FPGA (co-built with Eswin), focusing on the architectural understanding and development processes of domestic MCUs and FPGAs.

All core courses are paired with corresponding productive training courses, such as IC Layout Design Productive Training and IC Testing Productive Training, ensuring seamless connection between theory and practice.

2.3. Top-Layer Electives: Strengthening Cross-Border Integration and Innovative Practice

To cultivate composite talents, we set up 10 credits of professional elective courses and implement a "Primary-Secondary Job" mutual selection mechanism. After determining their primary job, apprentices must select one secondary job comprehensive practice course, such as Comprehensive Practice in Layout Design, Comprehensive Practice in IC Packaging and Testing, or Comprehensive Practice in IC Application Development. These courses are all high-intensity on-job practices of 64 class hours, led by partner enterprises. They focus on real engineering projects involving optical communication, memory, and MCUs, aiming to enhance apprentices' systemic thinking and cross-job collaborative capabilities.

3. Core Implementation: "One Student, One Pathway" Four-Stage Progressive Training Process

Based on the principles of "teaching according to aptitude, multi-job cognition, primary-secondary synergy, and job-enterprise adaptation," we designed a four-stage progressive training process spanning three years, with total practical teaching hours accounting for over 50%.

3.1. Stage 1: Foundation Consolidation (Semesters 1-2)

Objective: Solidify the foundation of theory and vocational literacy, and complete vocational cognition.

Implementation Content: All apprentices uniformly study public courses, professional foundation courses, and some professional core courses. Simultaneously, Professional Cognition Internship (1 week) and Labor Education Practice (1 week) are carried out. Students are organized to visit the "New Factory-in-School" and partner enterprises. Through lectures by corporate executives and sharing sessions by outstanding alumni, preliminary vocational cognition is established.

Key Measures: School-enterprise dual mentors establish growth files for each apprentice, tracking and recording learning performance to provide data support for subsequent job pre-selection.

3.2. Stage 2: Core Specialty Construction and Rotational Training (Semester 3)

Objective: Deepen core knowledge, experience the full-process craftsmanship, and clarify job intentions.

Implementation Content: Intensively study six professional core courses such as Fundamentals of IC Layout Design and Fundamentals of IC Packaging Technology. Simultaneously, enter the "Factory-in-School" to carry out rotational productive training. Apprentices rotate short-term (about 1 week per job) through training rooms for the five positions: layout, packaging, testing, facility management, and application development. They personally operate domestic EDA tools, ATE testers, wire bonders, and other equipment.

Key Measures: Through immersive rotation, apprentices comprehensively familiarize themselves with the workflows and skill requirements of each position. Combined with vocational assessments, they complete the pre-selection of primary and secondary jobs at the end of Semester 3.

3.3. Stage 3: Primary-Secondary Job Comprehensive Practice and Oriented Probation (Semester 4)

Objective: Refine primary job skills, expand secondary job capabilities, and achieve the transition to quasi-employees.

Path Implementation: Based on pre-selection results, implement the "1 Primary + 1 Secondary" training model.

Primary Job Deep Dive: For example, if "Layout Design" is chosen as the primary job, the apprentice deeply studies Comprehensive Practice in Layout Design (64 class hours). Under the guidance of Empyrean mentors, they complete the design and verification of complex modules such as operational amplifiers and bandgap reference circuits using domestic tools.

Secondary Job Synergy: If "Packaging and Testing" is chosen as the secondary job, they participate in Comprehensive Practice in IC Packaging and Testing (64 class hours) to understand the full process of packaging and testing for optical communication and memory chips, enhancing cross-job understanding.

Oriented Probation: An 8-week (160 class hours) oriented probation is conducted. Apprentices enter partner enterprises such as HX Microelectronics and Accotest as quasi-employees to undertake auxiliary tasks in a real production environment. Guided hand-in-hand by enterprise mentors, they achieve a "soft landing" from school to enterprise.

3.4. Stage 4: Enterprise Post Training and Graduation Standards (Semesters 5-6)

Objective: Independently take up posts and meet job competency standards.

Post Training: Apprentices formally enter their corresponding positions in enterprises to independently undertake production tasks or R&D projects for a duration of 24 weeks (384 class hours). School mentors conduct regular inspections, while enterprise mentors provide full-process guidance.

Graduation Design: Topics are sourced from actual technical problems in enterprises, implementing "real topics, real doing," such as "Optimization of Test Solutions for a Certain Model of Power Management Chip Based on Domestic ATE."

Exit Certification: Through an evaluation system of "Process Performance + Skill Certification + Comprehensive Portrait," those who meet the standards receive academic certificates, vocational skill level certificates, and enterprise micro-certificates, achieving "graduation equals employment."

4. Guarantee Mechanisms: Differentiated Assessment and Dynamic Adjustment

To ensure the effective implementation of "One Student, One Pathway," strict assessment and dynamic adjustment mechanisms have been established.

4.1. Differentiated Assessment of "Primary Core, Secondary Synergy"

Changing the traditional "one-size-fits-all" evaluation method, a weight allocation system is implemented: the primary job assessment weight is not less than 70%, focusing on core skill proficiency, independent working ability, and project outcome quality; the secondary job assessment weight is not more than 30%, focusing on collaborative working ability and auxiliary task completion. The assessment content covers multi-dimensional indicators including theoretical knowledge, job skills, and vocational literacy. The assessment methods integrate written exams, practical operations, enterprise project reviews, and mentor evaluations. The results serve as the direct basis for enterprise recruitment.

4.2. Path Dynamic Adjustment Mechanism

At the end of each semester, a joint school-enterprise assessment group conducts a comprehensive evaluation. If an apprentice shows incompatibility during rotation or primary-secondary job training (e.g., difficulty in mastering primary job skills but excellent performance in the secondary job), the primary and secondary job choices can be dynamically adjusted at the beginning of Semester 4. This is done upon judgment by dual mentors and with respect for the apprentice's willingness, ensuring maximized person-job matching.

4.3. Domestic Substitution Features Throughout the Process

All professional courses and training links are deeply implanted with domestic elements. For example, courses such as EDA Technology and Applications, Fundamentals of IC Layout Design, and Introduction to Verilog HDL and FPGA are explicitly labeled as "Domestic Substitution Featured Courses," mandating the use of domestic toolchains from Empyrean and Eswin for teaching. All training projects are derived from real cases of domestic chip enterprises, ensuring that students can immediately Capable of domestic production line work upon graduation.

5. Conclusion

The new apprenticeship training pathway for IC industry talents proposed in this paper is a systematic engineering project with the "New Factory-in-School" as the physical carrier, "One Student, One Pathway" as the logical guide, four-stage progressive real-post intensive training as the core means, and a differentiated evaluation mechanism as the guarantee. By reconstructing a modular curriculum system of 157.5 credits and deeply integrating resources from domestic leading enterprises such as Empyrean and Accotest, this pathway effectively solves the stubborn problems of disconnection between theory and practice, isolation between schools and enterprises, and lack of domestic tool application in traditional vocational education models.

This scheme not only achieves an organic connection between the education chain, talent chain, industry chain, and innovation chain but also highlights the strategic orientation of "domestic substitution," cultivating a large number of high-skilled talents proficient in domestic toolchains. It is estimated that after implementing this pathway, the targeted employment rate of graduates in relevant majors will stabilize above 95%, and the pre-job training cycle for new enterprise employees will be shortened by 60%. This model provides a highly operable "Suzhou Solution" and paradigm reference for talent training in IC and related strategic emerging industries at other vocational colleges.

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